

III) Please amend the ABSTRACT as set forth below:

5 A content addressable memory (CAM) device includes a plurality
 of memory-cell arrays for storing an array content therein provided for a
 data-access to an array based on a match with the array content. The
 CAM device further includes an error-check logic circuit connected to the
 memory-cell arrays for checking errors of the data access to each of the
 memory-cell arrays. The error-check logic circuit further includes an
10 array of identical parity-check circuit blocks represented by $P[i]$ where $i=1,$
 $2, 3, \dots, K$ and K is a positive integer and the identical parity-check circuit
 blocks performing a parity check on a rotational relationship with each of
 the $P[i]$ circuit block receiving input data from a $P[i-1]$ circuit block and
 sending output to a $P[i+1]$ circuit while the $P[K]$ circuit block sending
 output data to the $P[1]$ circuit block.

15 ~~This invention discloses a method for changing a configuring of an~~
 ~~error correction code (ECC) logic circuit for performing an error check of a~~
 ~~changed data width. The method includes the steps of: A) sequentially~~
 ~~interconnecting a set of $N1$ identical error check blocks where $N1$ is a first~~
20 ~~positive integer. And, the method further includes a step and B) of~~
 ~~reconfiguring the ECC logic circuit by changing the ECC logic circuit to a~~
 ~~set of $N2$ sequentially interconnected circuits comprising $N2$ of the~~
 ~~identical error check blocks where $N2$ is a second positive number. In a~~
 ~~preferred embodiment, the step of sequentially interconnecting a set of $N1$~~
25 ~~identical error check blocks is a step of interconnecting the $N1$ error check~~
 ~~blocks only between sequentially neighboring blocks for transmitting~~
 ~~signals only between the neighboring error check blocks. And, the step of~~
 ~~reconfiguring the ECC logic circuit by changing the ECC logic circuit to a~~
 ~~set of $N2$ sequentially interconnected circuits is a step of interconnecting~~
30 ~~the $N2$ error check blocks only between sequentially neighboring blocks~~
 ~~for transmitting signals only between the neighboring error check blocks.~~

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